29.3 A 1.2-to-8V Charge-Pump with Improved Power Efficiency for Non-Volatile Memories

A. Richelli[1], L. Mensi[1], L. Colalongo[1], P. L. Rolandi[2], Zs. M. Kovács-Vajna[1]

[1]University of Brescia, Brescia, Italy
[2]STMicroelectronics, Milan, Italy

Low-voltage circuit technologies for processors, memories and I/O circuits are intensively used today. Systems-on-a-chip based on these technologies often use high-density flash memories. Despite the power supply trends, flash memories, as well as EEPROM and OTP memories, still require high internal voltages of about 6 to 8V in order to activate tunnelling and hot-electron injection during both writing and erasing operations. Charge pumps based on the Dickson architecture are widely used and provide approximately a maximum output voltage equal to $(N + 1)\cdot(V_{dd} - V_T)$, where N is the number of stages, V_{dd} is the supply voltage and V_T is the threshold voltage of the diode-connected MOS transistors. The main drawbacks of this architecture come from the V_T drop and from the body effect. Since V_T cannot be scaled as much as the scaling trend of the supply voltage, the impact of the threshold voltage becomes more appreciable in recent low-voltage technologies. Therefore, several attempts have been made to reduce the V_T loss and the body effect, and increase the power efficiency [1-5], and a lot of work has been devoted to clarify the power consumption of the charge pumps [6]. In [6] a charge pump is considered based on ideal switches, instead of pass-transistors, and a simple expression for the power efficiency η is found, focusing on the efficiency reduction caused by the bottom plate parasitics of the boost capacitors:

$$\eta = \frac{I_L \cdot V_{out}}{I_{power} \cdot V_{dd}} \qquad (1)$$

where N is the number of stages, I_L is the current delivered to the load, and I_{power} is the current delivered by the voltage supply to the pump, which also accounts for the current loss, I_s, needed to charge and discharge the parasitic capacitors. The overall wasted current can be written as:

$$I_{power} = (N+1)\cdot I_L + I_s \qquad (2) \quad \text{and} \quad I_s = N \cdot C_p \cdot f \cdot V_{dd} \qquad (3)$$

where C_p is the parasitic capacitance of the boost capacitor and is proportional to the boost capacitance itself by a factor α:

$$I_s = \alpha \cdot N \cdot C \cdot f \cdot V_{dd} \qquad (4)$$

Therefore, the power efficiency may be rewritten as:

$$\eta = \frac{I_L \cdot V_{out}}{I_{power} \cdot V_{dd}} = \frac{\frac{V_{out}}{V_{dd}}}{N+1+\alpha \cdot \frac{N^2}{N+1-\frac{V_{out}}{V_{dd}}}} \qquad (5)$$

The α parameter is technology dependent, varying between 0.1 (for poly-poly capacitors) and 0.4 (for other capacitors like metal-metal capacitors).

The power efficiency of an 8-stage charge pump is shown in Fig. 29.3.1 as a function of the current delivered to the load for $\alpha = 0.1$ and 0.3. The curves also show how the efficiency is reduced by taking into account the 10kΩ switch resistances. Following the approach in [6], simulations have been performed considering only the parasitic capacitances of the boost capacitors and neglecting other losses (such as, for example, the parasitic components of the pass-transistors). It is worth noting that even assuming ideal pass-transistors, the maximum power efficiency is less than 50% and is reduced by increasing α and, obviously, by increasing switch resistances.

In this paper a new charge pump architecture is presented that exhibits improved power efficiency and a high-voltage output. The increased power efficiency compared to the known Dickson architectures is obtained by partially reusing the charge on the capacitors. The charge transfer block of the charge pump is shown in Fig. 29.3.2: it is based on two blocks (namely Block *P* and Block *N*), regulated by two complementary clock signals (*Clk* and $\overline{Clk}$); CTM_p and CTM_n are the pass-transistors of blocks *P* and *N*, respectively. The active control of *CTM*'s body voltage is based on two auxiliary devices, P_1 and P_2 for CTM_p, and N_1 and N_2 for CTM_n, as explained in [2]. Furthermore, a new dynamic control of *CTM's* gate voltage is provided by the auxiliary transistors P_p (for CTM_p) and N_p (for CTM_n) and the voltage drop V_T of the pass-transistors is drastically reduced leading to a nearly full V_{dd} step for each stage. The reason why a complete V_{dd} step cannot be achieved in the final charge pump is that the boost capacitor is charged through the switch resistance, leading to incomplete charging over the finite clock period.

When $Clk = 0$ and $\overline{Clk} = V_{DD}$, P_p turns *ON*, the gate and source of CTM_p are shorted and CTM_p is *OFF*; on the other hand, CTM_n is *ON* and the charge can be moved from the boost capacitors $C_{(n-1)d}$ and C_{nd}. Similarly, when $Clk = V_{DD}$ and $\overline{Clk} = 0V$, the charge can be transferred from $C_{(n-1)u}$ to C_{nu}.

The main advantages of this architecture derive from the reduced equivalent resistance of *CTM*, which is half what it is in state-of-the art charge pumps [4] based on the Favrat cell, and from the charge recycling capability. In order to clarify this point, the current flow when CTM_p is OFF and CTM_n is *ON* is shown in Fig. 29.3.2 by the arrows. In this condition, along with the charge transfer from $C_{(n-1)d}$ to C_{nd}, some charge is stored on the gates of CTM_p and CTM_n. During the next clock pulse, this charge itself increases the voltage boost.

Figure 29.3.3 shows, with a black line and stars, the efficiency as a function of the output current for a 10-stage charge pump designed in a 130nm CMOS process using poly-poly capacitors. The simulated efficiency is almost always higher then the best ideal performance thanks to the charge recycling capability.

Figure 29.3.3 shows the power efficiencies as functions of the output current for different numbers of stages. It is worth noting that increasing the number of stages increases the power efficiency as well. This is the real case of technology evolution where the output voltage is fixed by the physical phenomenon to be 6 to 8V, while the power supply decreases forcing more and more stages.

In order to confirm the validity of this new architecture by measurements, the charge pump was fabricated using a 130nm CMOS process, but only a technology without poly-poly capacitors was available. Therefore, metal-metal capacitors were used and α is around 0.3 in this case, which reduces the efficiency significantly. In order to evaluate the charge pump behaviour (maximum output voltage, power efficiency and die area), an 8-stage pump was used and and optimized for a current of 120μA delivered to the load, as shown in Fig. 29.3.4.

Several cycles of measurements for many chips were performed using the nominal working conditions (1.2V voltage supply and 100MHz clock) with a resistive load ranging from 30 to 80kΩ connected to the output. The output voltage and power efficiency are shown in Figures 29.3.5 and 29.4.6, respectively. Thanks to the charge recycling capability, the power efficiency is larger than the efficiency of a charge pump in the same operating condition, based on ideal switches as shown in Fig. 29.3.1. Since the measurements confirm the simulations of the architecture using metal-metal capacitors, it is reasonable to assume that a design employing poly-poly capacitors can achieve a power efficiency close to the topmost curve shown in Fig. 29.3.1, which represents an improvement of more than 25% when compared to the Favrat-cell-based charge pumps [4] with the same measurement conditions. The core area of the proposed 8-stage charge pump is 300μm×100μm.

Acknowledgments:
The authors wish to thank STMicroelectronics for the foundry service and for the help provided by D. Lena, M. Poles and L. Fumagalli at Central Cad & Design Solutions, STMicroelectronics, Agrate (Milan), Italy.

References:
[1] K.H. Cheng, C.-Y. Chang and C.-H. Wei, "A CMOS Charge Pump for Sub-2.0V Operation," *ISCAS*, Vol. 5, pp. V89-V92, 2003.
[2] J. Shin et al., "A New Charge Pump Without Degradation in Threshold Voltage due to Body Effect," *IEEE J. Solid-State Circuits*, pp. 1227-1230, Aug., 2000.
[3] J. T. Wu et al., "MOS Charge Pumps for Low-Voltage Operation," *IEEE J. Solid-State Circuits*, pp. 592-597, Apr., 1998.
[4] R. Pelliconi et al., "Power Efficient Charge Pump in Deep Submicron Standard CMOS Technology," *IEEE J. Solid-State Circuits*, pp. 1068-1071, June, 2003.
[5] L. Mensi et al., "A New Integrated Charge Pump Architecture using Dynamic Biasing of Pass-Transistors," *Proc. ESSCIRC*, pp. 85-88, 2005.
[6] G. Palumbo, D. Pappalardo and M. Gaibotti, "Charge-Pump Circuits: Power-Consumption Optimization," *IEEE T. CAS I*, pp. 1535-1542, Nov., 2002.

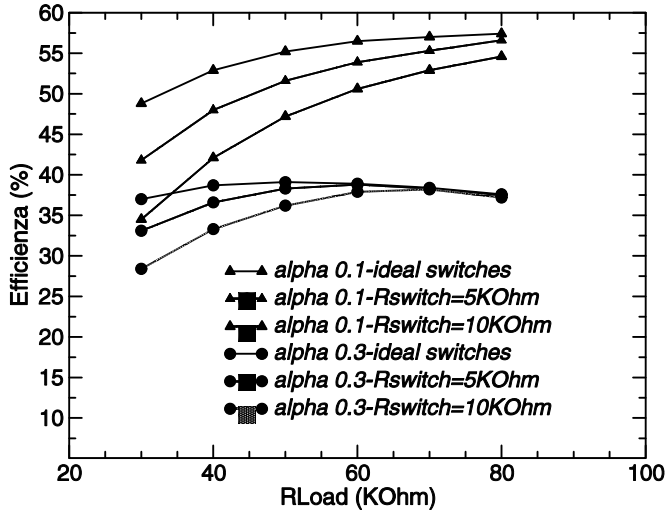

Figure 29.3.1: Power efficiency verses I_{outs} as a function of α.

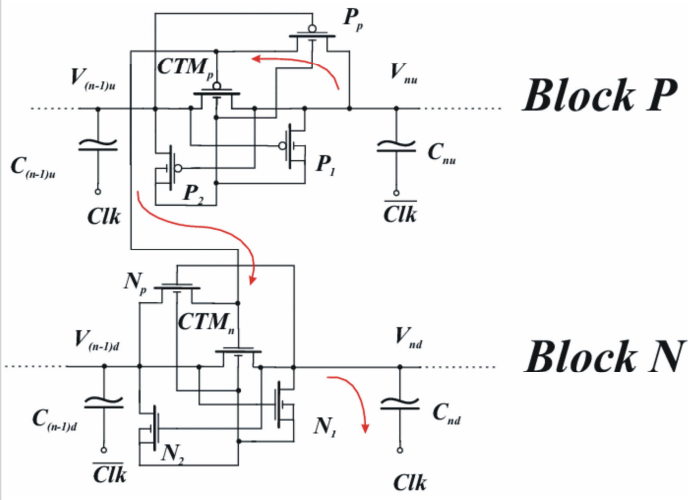

Figure 29.3.2: Charge transfer blocks of the architecture and current flow explaining the charge recycling capability.

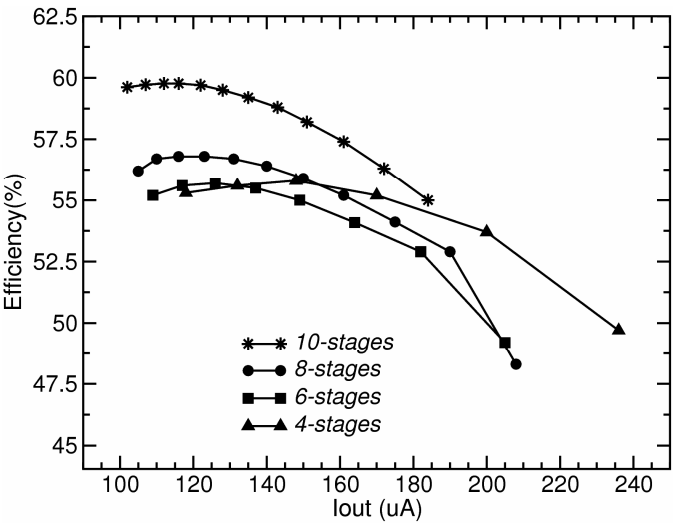

Figure 29.3.3: Power efficiency verses I_{outs} as a function of the number of stages.

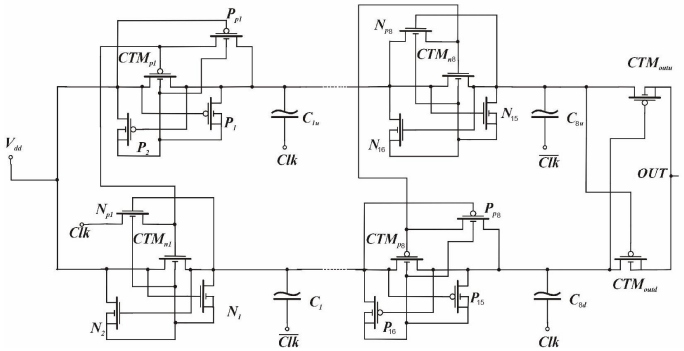

Figure 29.3.4: Schematic of the 8-stage charge pump .

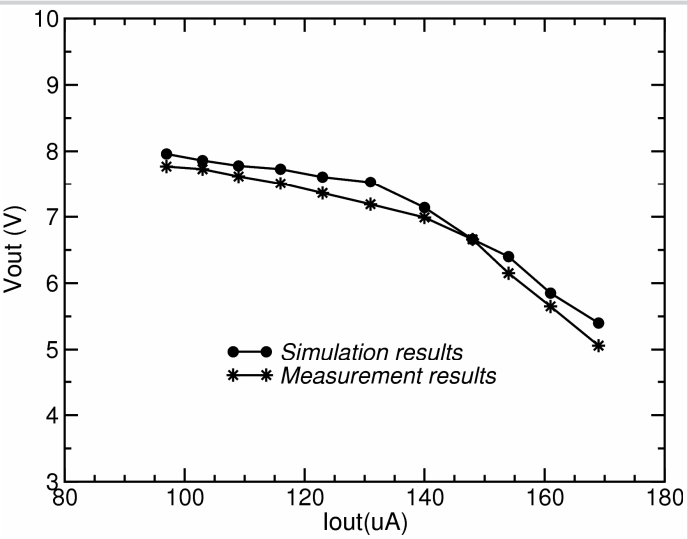

Figure 29.3.5: Simulated and measured output voltage as a function of the output current.

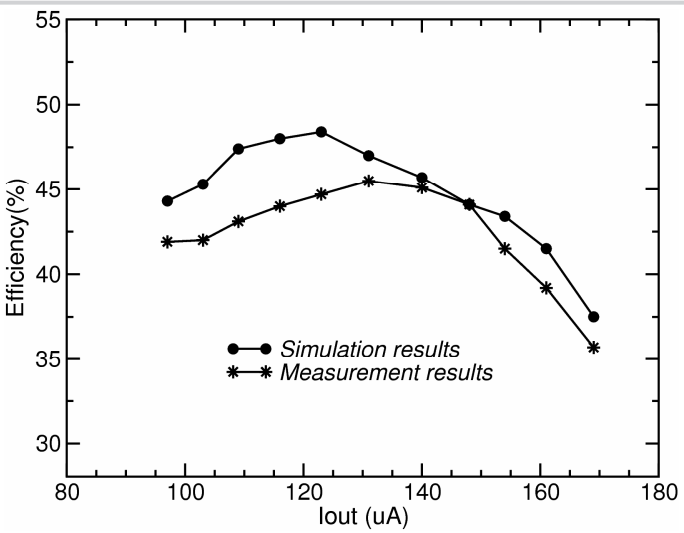

Figure 29.3.6: Simulated and measured power efficiency as a function of the output current.

Continued on Page 619

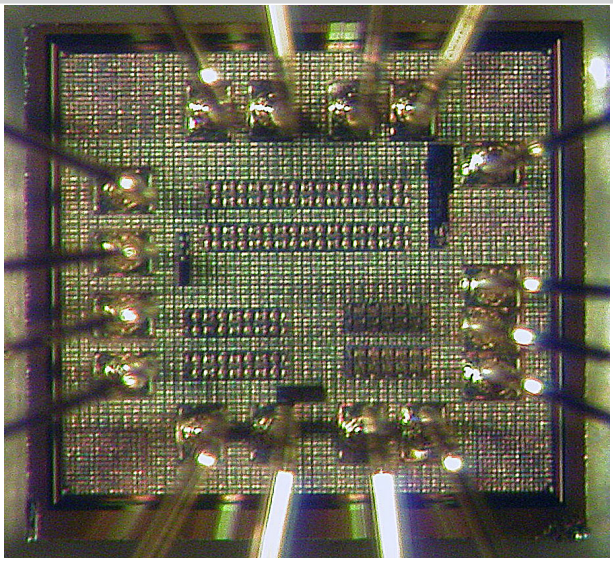

Figure 29.3.7: Chip micrograph.

